AMENDMENTS TO THE CLAIMS

Please cancel claims 1, 5, 9, 16, 18, 20, 22, 24, 50, and 59 and amend claims 2, 4, 6, 8, 10, 11, 13, 14, 15, 17, 19, 21, 23, 25, 26, 28, 30, 32, 34, 38, 43, 44, 45, 46, 48, 51, 53-58, 60, and 62-67 as set forth below.

1. (CANCELED)

2. (CURRENTLY AMENDED) An arithmetic device as set forth in ~~claim 1~~ claim 4, wherein the arithmetic means performs dyadic operation.

3. (ORIGINAL) An arithmetic device as set forth in claim 2, wherein the arithmetic means performs monadic operation on the result of the dyadic operation.

4. (CURRENTLY AMENDED) An arithmetic device ~~as set forth in claim 1, further comprising~~ that reconfigures an operation path by outside control, comprising:

first selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

second selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

arithmetic means receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operations in accordance with instructions of a control signal; and

[[a]] delay means for outputting the input data delayed by an amount of delay according to a control signal.

5. (CANCELED)

6. (CURRENTLY AMENDED) An arithmetic device as set forth in ~~claim 5~~ claim 8, wherein the arithmetic means performs trinomial operation.

7. (ORIGINAL) An arithmetic device as set forth in claim 6, wherein the arithmetic means performs monadic operation on the result of the trinomial operation.

8. (CURRENTLY AMENDED) An arithmetic device ~~as set forth in claim 5, further comprising~~ that reconfigures an operation path by outside control, comprising:

first selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

second selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

third selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

arithmetic means receiving as input the output signal of the first selecting means, the output signal of the second selecting means, and the output signal of the third selecting means and performing operation in accordance with instructions of a control signal; and

[[a]] delay means for outputting the input data delayed by an amount of delay according to a control signal.

9. (CANCELED)

10. (CURRENTLY AMENDED) An arithmetic device as set forth in ~~claim 9~~ claim 13, further comprising a fourth selecting means for selecting one of the output signal of the first arithmetic means and the output signal of the second arithmetic means in accordance with a control signal.

11. (CURRENTLY AMENDED) An arithmetic device as set forth in ~~claim 9~~ claim 13, wherein the first arithmetic means performs dyadic operation, while the second arithmetic means performs trinomial operation.

12. (ORIGINAL) An arithmetic device as set forth in claim 11, wherein the first arithmetic means performs monadic operation on the result of the dyadic operation, while the second arithmetic means performs monadic operation on the result of the trinomial operation.

13. (CURRENTLY AMENDED) An arithmetic device ~~as set forth in claim 9, further comprising~~ that reconfigures an operation path by outside control, comprising:

first selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

second selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

third selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

first arithmetic means receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal;

second arithmetic means receiving as input the output signal of the first selecting means and the output signal of the second selecting means and third selecting means and performing operation in accordance with instructions of a control signal; and

[[a]] delay means for outputting the input data delayed by an amount of delay according to a control signal.

14. (CURRENTLY AMENDED) An arithmetic device able to reconfigure operation path by outside control, comprising:

a first selecting means for selecting from a first data group in accordance with a control signal,

a second selecting means for selecting one from a second data group in accordance with a control signal,

a first arithmetic means for receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal,

a second arithmetic means for receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal, [[and]]

a third selecting means for selecting one of the output signal of the first arithmetic means and the output signal of the second arithmetic ~~means~~ means; and

delay means for outputting the input data delayed by an amount of delay according to a control signal.

15. (CURRENTLY AMENDED) An arithmetic device able to reconfigure an operation path by outside control, comprising:

a first selecting means for selecting one data from a first data group in accordance with a control signal,

a second selecting means for selecting one data from a second data group in accordance with a control signal,

a third selecting means for selecting one data of a third data group in accordance with a control signal,

a first arithmetic means for receiving as input at least two signals among the output signal of the first selecting means, the output signal of the second selecting means, and the output signal of the third selecting means and performing operation in accordance with instructions of a control signal,

a second arithmetic means for receiving as input at least two signals among the output signal of the first selecting means, the output signal of the second selecting means, and the output signal of the third selecting means and performing operation in accordance with instructions of a control signal, [[and]]

a fourth selecting means for selecting one of the output signal of the first arithmetic means and the output signal of the second arithmetic ~~means~~ means; and

delay means for outputting the input data delayed by an amount of delay according to a control signal.

16. (CANCELED) A parallel arithmetic device having a plurality of arithmetic devices, each comprising:

a first selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a second selecting means for selecting desired data from a plurality of input data in accordance with a control signal, and

an arithmetic means receiving as input the output signal of the first selecting means and the output signal of the second selecting means in accordance with a control signal and

able to reconfigure an operation path by outside control,

connects the inputs and outputs of data of the plurality of arithmetic devices in cascade, and

supplies the operation result signal of an arithmetic device as one data of a plurality of data inputs of another device.

17. (CURRENTLY AMENDED) A parallel arithmetic device ~~as set forth in claim 16, further comprising~~ having a plurality of arithmetic devices, each comprising:

first selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

second selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

arithmetic means for receiving as an input the output signal of the first selecting means and the output signal of the second selecting means in accordance with a control signal;

configuration means for reconfiguring an operation path by outside control;

connection means for connecting the inputs and outputs of data of the plurality of arithmetic devices in cascade;

supply means for supplying the operation result signal of an arithmetic device as one of a plurality of data inputs of another device; and

[[a]] delay means for delaying the input data by an amount of delay in accordance with a control signal and outputting it to the arithmetic device of the next stage.

18. (CANCELED)

19. (CURRENTLY AMENDED) A parallel arithmetic device ~~as set forth in claim 18, further comprising~~ having a plurality of arithmetic devices, each comprising:

a first selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

a second selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

a third selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

an arithmetic means for receiving as input the output signal of the first selecting means, the output signal of the second selecting means, and the output signal of the third selecting means, and performing an operation in accordance with instructions of a control signal;

configuration means for reconfiguring an operation path under outside control;

connection means for connecting in cascade the inputs and outputs of data of the plurality of arithmetic devices;

supply means for supplying the operation result signal of an arithmetic device as one data of the plurality of data inputs of another device; and

a delay means for delaying the input data by an amount of delay in accordance with a control signal and outputting it to the arithmetic device of the next stage.

20. (CANCELED)

21. (CURRENTLY AMENDED) A parallel arithmetic device ~~as set forth in claim 20, further comprising~~ having a plurality of arithmetic devices, each comprising:

a first selecting means for selecting desired data from a plurality of input-data in accordance with a control signal;

a second selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

a third selecting means for selecting desired data from a plurality of input data in accordance with a control signal;

a first arithmetic means for receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal;

a second arithmetic means for receiving as an input the output signal of the first selecting means, the output signal of the second selecting means, and the output signal of the third selecting means and performing operation in accordance with instructions of a control signal;

a fourth selecting means for selecting one of the output of the first arithmetic means and the output of the second arithmetic means in accordance with a control signal and outputting the same as an operation result signal;

configuration means for reconfiguring an operation path under outside control;

connection means for connecting in cascade the inputs and outputs of data of the plurality of arithmetic devices, and

supply means for supplying the operation result signal of one of the plurality of arithmetic devices as one of the plurality of data inputs of another device; and

a delay means for delaying the input data by an amount of delay in accordance with a control signal and outputting it to the arithmetic device of the next stage.

22. (CANCELED)

23. (CURRENTLY AMENDED) A parallel arithmetic device ~~as set forth in claim 22, further comprising~~ having a plurality of arithmetic devices, each comprising:

a first selecting means for selecting one data from a first data group in accordance with a control signal;

a second selecting means for selecting one data from a second data group in accordance with a control signal;

a first arithmetic means receiving as an input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal;

a second arithmetic means receiving as an input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal;

a third selecting means for selecting an output of the first arithmetic means and an output of the second arithmetic means in accordance with a control signal and outputting the same as an operation result signal;

configuration means for reconfiguring an operation path under outside control;

connection means for connecting in cascade the inputs and outputs of data of the first data group of the plurality of arithmetic devices;

supply means for supplying the operation result signal of an arithmetic device as data of a second data group of another device; and

a delay means for delaying the first data group by an amount of delay in accordance with a control signal and outputting it to the arithmetic device of the next stage.

24. (CANCELED)

25. (CURRENTLY AMENDED) A parallel arithmetic device ~~as set forth in claim 24 further comprising~~ having a plurality of arithmetic devices, each comprising:

a first selecting means for selecting one data from a first data group in accordance with a control signal;

a second selecting means for selecting one data from a second data group in accordance with a control signal;

a third selecting means for selecting one from a third data group in accordance with a control signal;

a first arithmetic means receiving as input at least two signals of the output signal of the first selecting means, the output signal of the second selecting means, and the output signal of the third selecting means and performing operation in accordance with instructions of a control signal;

a second arithmetic means receiving as input at least two signals of the output signal of the first selecting means, the output signal of the second selecting means, and the output signal of the third selecting means and performing operation in accordance with instructions of a control signal;

a fourth selecting means for selecting one of the output of the first arithmetic means and the output of the second arithmetic means in accordance with a control signal;

configuration means for reconfiguring an operation path under outside control;

connection means for connecting in cascade the inputs and outputs of data of the first data group and the second data group of the plurality of arithmetic devices;

supply means for supplying the operation result signal of an arithmetic device as one data of a third data group of another device;

a first delay means for outputting the first data group to the arithmetic device of the next stage delayed by an amount of delay in accordance with a control ~~signal~~ signal; and

a second delay means for outputting the second data group to the arithmetic device of the next stage delayed by exactly an amount of delay in accordance with a control signal.

26. (CURRENTLY AMENDED) An arithmetic device reconfigurable by outside control, comprising:

at least one computing unit having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal and outputting the operation ~~results and~~ results;

a plurality of input selection devices for selecting one data from the plurality of input data in accordance with a control signal and supplying the same to different inputs of the computing ~~unit~~unit; and

a delay unit that delays and outputs the plurality of outputs of the at least one computing unit based on a control signal.

27. (ORIGINAL) An arithmetic device as set forth in claim 26, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of input data and supplying the operation results to one input of the input selection device.

28. (CURRENTLY AMENDED) An arithmetic device reconfigurable by outside control, comprising:

at least one multiple input, multiple output computing unit each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of ~~outputs and~~ outputs;

a plurality of output selection devices for selecting and outputting one data from the plurality of input data and the output data of the computing unit in accordance with a control ~~signal~~signal; and

a delay unit that delays and outputs the plurality of outputs of the at least one multiple input, multiple output computing unit based on a control signal.

29. (ORIGINAL) An arithmetic device as set forth in claim 28, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of input data and supplying the operation results to the output selection device.

30. (ORIGINAL) An arithmetic device reconfigurable by outside control, comprising:

at least one computing unit having a plurality of inputs and a plurality of outputs, performing a plurality of operations based an data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the computing unit, ~~and~~

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and the output data of the computing unit in accordance with a control ~~signal~~ signal; and

a delay unit that delays and outputs the plurality of outputs of the at least one computing unit based on a control signal.

31. (ORIGINAL) An arithmetic device as set forth in claim 30, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data among the plurality of input data and supplying operation results to one input of the input selection devices and the output selection device.

32. (CURRENTLY AMENDED) An arithmetic device reconfigurable by outside control, comprising:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying the same to different inputs of the first computing units, ~~and~~

at least one second computing unit having a plurality of inputs and a plurality of outputs, supplied at the plurality of inputs with output data of the plurality of first computing units, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of ~~outputs~~ outputs,

a delay unit that sets a delay between the first and second computing units based on a control signal.

33. (ORIGINAL) An arithmetic device as set forth in claim 32, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of input data and supplying the operation results to one input of the input selection device.

34. (CURRENTLY AMENDED) An arithmetic device reconfigurable by outside control, comprising:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

at least one second computing unit having a plurality of inputs and a plurality of outputs, supplied at the plurality of inputs with output data of the plurality of first computing units, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of ~~outputs, and~~ outputs; and

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and the output data of at least one of the first and second computing ~~units~~ units;

a delay unit that sets a delay between the first and second computing units based on a control signal.

35. (ORIGINAL) An arithmetic device as set forth in claim 34,wherein the plurality of output selection devices include:

a plurality of first output selection devices for selecting and outputting one data from a plurality of input data and output data of the first computing unit in accordance with a control signal and

a plurality of second output selection devices selecting and outputting one data from a plurality of input data, the output data of the first computing unit, and the output data of the second computing unit in accordance with a control signal.

36. (ORIGINAL) An arithmetic device as set forth in claim 34, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of input data and supplying the operation results to the output selection device.

37. (ORIGINAL) An arithmetic device as set forth in claim 35, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of input data and supplying the operation results to the first output selection device.

38. (CURRENTLY AMENDED) An arithmetic device reconfigurable by outside control, comprising:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of input selection devices for selecting one data from the plurality of input data in accordance with a control signal and supplying the same to different inputs of the first computing units,

at least one second computing unit each having a plurality of inputs and a plurality of outputs, supplied at the plurality of inputs with the output data of the plurality of first computing units, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of ~~outputs, and~~ outputs; and

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and at least one output data among the first and second computing units in accordance with a control ~~signal~~signal; and

a delay unit that sets a delay between the first and second computing units based on a control signal.

39. (ORIGINAL) An arithmetic device as set forth in claim 38, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of input data and supplying the operation results to one input of the input selection device.

40. (ORIGINAL) An arithmetic device as set forth in claim 38, wherein the plurality of output selection devices include

a plurality of first output selection devices each selecting and outputting one data from a plurality of input data and the output data of the first computing unit in accordance with a control signal and

a plurality of second output selection devices each selecting and outputting one data from the plurality of input data, the output data of the first computing unit, and the output data of the second computing unit in accordance with a control signal.

41. (ORIGINAL) An arithmetic device as set forth in claim 38, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of input data and supplying the operation results to the output selection device.

42. (CURRENTLY AMENDED) An arithmetic device as set forth in claim 40, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of ~~Input~~ input data and supplying the operation results to the first output selection device.

43. (CURRENTLY AMENDED) An arithmetic device reconfigurable by outside control, comprising:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of first input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying the same to different inputs of the first computing units,

at least one second computing unit each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on a plurality of data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of ~~outputs, and~~ outputs; and

a plurality of second input selection devices each selecting one data from the plurality of input data and the output data of the second computing units in accordance with a control signal and supplying it to different inputs of the second computing ~~unit~~ unit; and

a delay unit that sets a delay between the first and second computing units based on a control signal.

44. (ORIGINAL) An arithmetic device reconfigurable by outside control, comprising:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of first input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it todifferent inputs of the first computing units,

at least one second computing unit having a plurality of inputs and a plurality of outputs,

performing a plurality of operations based on a plurality of data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of second input selection devices for selecting one data from the plurality of input data and the output data of the second computing unit in accordance with a control signal and supplying it to different inputs of the second computing ~~unit, and~~ unit;

a plurality of output selection devices each selecting and outputting one data from a plurality of input data and at least one output data of the second computing unit in accordance with a control ~~signal~~ signal; and.

a delay unit that sets a delay between the first and second computing units based on a control signal

45. (CURRENTLY AMENDED) An arithmetic device reconfigurable by outside control, comprising:

a plurality of computing units, arranged in multiple stages, each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of ~~outputs and~~ outputs;

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the plurality of computing units of the first ~~stage,~~ stage; and

a delay unit that delays and outputs the plurality of outputs to a next stage based on a control signal,

the computing units arranged in stages other than the computing units of the first stage each being supplied at the plurality of inputs with output data of the plurality of computing units of the previous stage, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs.

46. (CURRENTLY AMENDED) An arithmetic device reconfigurable by outside control, comprising:

a plurality of computing units, arranged in multiple stages, each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of ~~outputs and~~ outputs;

a plurality of output selection devices each selecting and outputting one data from a plurality of input data and at least one output data of the computing units of the each stage in accordance with a control ~~signal,~~ signal; and

a delay unit that delays and outputs the plurality of outputs to a next stage based on a control signal,

the computing units arranged in the stages other than the computing units of the first stage each being supplied at the plurality of inputs with output data of the plurality of computing units of the previous stage, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs.

47. (ORIGINAL) An arithmetic device as set forth in claim 46, wherein the plurality of output selection devices include

a plurality of first output selection devices each selecting and outputting one data from a plurality of input data and the output data of the computing unit of the first stage in accordance with a control signal and

a plurality of second output selection devices each selecting and outputting one data from the plurality of input data and the output data of the computing units of the different stages in accordance with a control signal.

48. (CURRENTLY AMENDED) An arithmetic device reconfigurable by outside control, comprising:

a plurality of computing units, arranged in multiple stages, each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on the data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the plurality of computing units of the first ~~stage, and~~ stage;

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and at least one output data among the computing units of stages in accordance with a control ~~signal,~~ signal; and

a delay unit that delays and outputs the plurality of outputs to a next stage based on a control signal,

the computing units arranged in the stages other than the computing units of the first stage each being supplied at the plurality of inputs with the output data of the plurality of computing units of the previous stage, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs.

49. (ORIGINAL) An arithmetic device as set forth in claim 48, wherein the plurality of output selection devices include

a plurality of first output selection devices each selecting and outputting one data from a plurality of input data and the output data of the computing unit of the first stage in accordance with a control signal and

a plurality of second output selection devices each selecting and outputting one data from the plurality of input data and the output data of the computing units of the different stages in accordance with a control signal.

50. (CANCELED)

51. (CURRENTLY AMENDED) A parallel arithmetic device as set forth in ~~claim 50~~ claim 58, wherein the first arithmetic device includes:

a first selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a second selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a third selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a first arithmetic means receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal, and

a second arithmetic means receiving as input the output signal of the first selecting means and the output signals of the second selecting means a third selecting means and performing operation in accordance with instructions of a control signal.

52. (ORIGINAL) A parallel arithmetic device as set forth in claim 51, wherein the first arithmetic device further comprises a fourth selecting means for selecting one of the output signal of the first arithmetic means and the output signal of the second arithmetic means in accordance with a control signal.

53. (CURRENTLY AMENDED) A parallel arithmetic device as set forth in ~~claim 50~~ claim 58, wherein the first arithmetic device includes a plurality of arithmetic devices and connects the inputs and outputs of data of the plurality of arithmetic devices in cascade and supplies the operation result signal of an arithmetic device as one data of a plurality of data inputs of another device.

54. (CURRENTLY AMENDED) A parallel arithmetic device as set forth in ~~claim 50~~ claim 58, wherein the second arithmetic device comprises:

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the computing unit and

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and the output data of the computing unit in accordance with a control signal.

55. (CURRENTLY AMENDED) A parallel arithmetic device as set forth in ~~claim 50~~ claim 58, wherein the second arithmetic device includes:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the find computing unit, and

at least one second computing unit having a plurality of inputs and a plurality of outputs, supplied at the plurality of inputs with output data of the plurality of first computing units, performing a plurality of operations based on the supplied plurality of data in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and at least one output data of the first and second computing units in accordance with a control signal.

56. (CURRENTLY AMENDED) A parallel arithmetic device as set forth in ~~claim 50~~claim 58, wherein the second arithmetic device includes:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of first input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the first computing unit, and

at least one second computing unit having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on the plurality of data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of second input selection devices each selecting one data from the plurality of input data and the output data of the second computing units and supplying it to different inputs of the second computing units, and

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and at least one output data of the second computing units in accordance with a control signal.

57. (CURRENTLY AMENDED) A parallel arithmetic device as set forth in ~~claim 50~~ claim 58, wherein the second arithmetic device includes:

a plurality of computing units, arranged in multiple stages, each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on the data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the plurality of computing units of the first stage, and

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and at least one output data among the computing units of stages in accordance with a control signal, the computing units arranged in the stages other than the computing units of the first stage each being supplied at the plurality of inputs with the out put data of the plurality of computing units of the previous stage, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs.

58. (CURRENTLY AMENDED) A parallel arithmetic device ~~as set forth in claim 50, further comprising~~ comprising:

a first arithmetic device reconfigurable by outside control having at least two selecting means each selecting desired data from a plurality of input data in accordance with a control signal and at least one arithmetic device including at least one arithmetic means for receiving output signals of the selecting means and performing operation in accordance with instructions of a control signal;

a second arithmetic device reconfigurable by outside control including at least one computing unit having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs; and

[[a]] delay means ~~able to set~~ for setting any delay between the arithmetic ~~devices~~ devices,

the operation results of at least one of the first arithmetic device and second arithmetic device being supplied as input data of the other arithmetic device.

59. (CANCELED)

60. (CURRENTLY AMENDED) A parallel arithmetic device as set forth in ~~claim 59~~ claim 67, wherein the first arithmetic device includes:

a first selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a second selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a third selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a first arithmetic means for receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal, and

a second arithmetic means for receiving as input the output signal of the first selecting means and the output signals of the second selecting means and third selecting means and performing operation in accordance with instructions of a control signal.

61. (ORIGINAL) A parallel arithmetic device as set forth in claim 60, wherein the first arithmetic device further comprises a fourth selecting means for selecting one of the first arithmetic means and the output signal of the second arithmetic means in accordance with a control signal.

62. (CURRENTLY AMENDED) A parallel arithmetic device as set forth in ~~claim 59~~ claim 67, wherein the first arithmetic device includes a plurality of arithmetic devices, connects

in cascade the inputs and outputs of data of the plurality of arithmetic devices, and supplies the operation result signal of each arithmetic device as one data of the plurality of data inputs of another device.

63. (CURRENTLY AMENDED) A parallel arithmetic device as set forth in ~~claim 59~~ claim 67, wherein the second arithmetic device comprises:

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the computing unit and

a plurality of output selection devices a selecting and outputting one data from the plurality of input data and the output data of the computing unit of accordance with a control signal.

64. (CURRENTLY AMENDED) A parallel arithmetic device as set forth in ~~claim 59~~ claim 67, wherein the second arithmetic device includes:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the first computing units,

at least one second computing unit each having a plurality of inputs and a plurality of outputs, supplied at the plurality of inputs with output data of the plurality of first computing units, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs, and

a plurality of output selection devices each selecting and outputting one data from a plurality of input data and at least one output data of the first and second computing units in accordance with a control signal.

65. (CURRENTLY AMENDED) A parallel arithmetic device as set forth in ~~claim 59~~ claim 67, wherein the second arithmetic device includes

a plurality of first computing units each in having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of first input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the first computing units,

at least one second computing unit each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on the plurality of data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of second input selection devices each selecting one data from the plurality of input data and output data of the second computing unit in accordance with a control signal, and

a plurality of output selection devices each selecting and outputting one data from a plurality of input data and at least one output data of the second computing unit in accordance with a control signal.

66. (CURRENTLY AMENDED) A parallel arithmetic device as set forth in ~~claim 59~~ claim 67, wherein the second arithmetic device includes:

a plurality of computing units, arranged in, multiple stages, each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of, inputs in accordance with a control signal and outputting the operation results from the plurality of outputs,

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the computing units of the first stage, and a plurality of output selection devices each selecting and outputting one data from a plurality of input data and at least one output data of the computing units of the stages in accordance with a control signal,

the computing units arranged in stages other than the computing units of the first stage each being supplied at the plurality of inputs with output data of the plurality of computing units of the previous stage performing a plurality of operations based on the plurality of data

supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs.

67. (CURRENTLY AMENDED) A parallel arithmetic device ~~as set forth in claim 59, further comprising~~ comprising:

a plurality of first arithmetic devices reconfigurable by outside control each having at least two selecting means each selecting desired data from plurality of input data in accordance with a control signal and at least one arithmetic device including at least one arithmetic means for receiving output signals of the selecting means and performing operation in accordance with instructions of a control signal;

a plurality of second arithmetic devices reconfigurable by outside control each including at least one computing unit each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs, the operation results of the plurality of first arithmetic devices being supplied to the corresponding second arithmetic devices and the operation results of the second arithmetic devices being supplied to the corresponding first arithmetic devices; and

a delay means ~~able to set~~ for setting any delay between arithmetic devices.

68-109. (CANCELED)